UM2218
User manual

STuW81300-EVB evaluation board and STSW-RFSOL003 software for STuW81300

Introduction

The STuW81300-EVB evaluation board and its dedicated software with a graphical user interface (STSW-RFSOL003) allow the user to program and operate the STuW81300 Wideband RF/Microwave PLL fractional/integer frequency synthesizer and its integrated VCOs and LDOs.

The PC-compatible software with GUI allows the user to write and read all device registers. This gives direct control of circuit functions such as operating frequency, reference frequency, input mode, charge pump current and low-power modes.

The GUI is user-oriented to aid understanding of the performance, features and characteristics of the STuW81300 device under test in a laboratory environment. The GUI instantly shows descriptions of its controls and indicators when the user hovers the mouse cursor over them.

This user manual provides the information needed to start using the STuW81300-EVB board and the STSW-RFSOL003 software. Board electrical schematic diagrams and a full bill-of-materials are also included.

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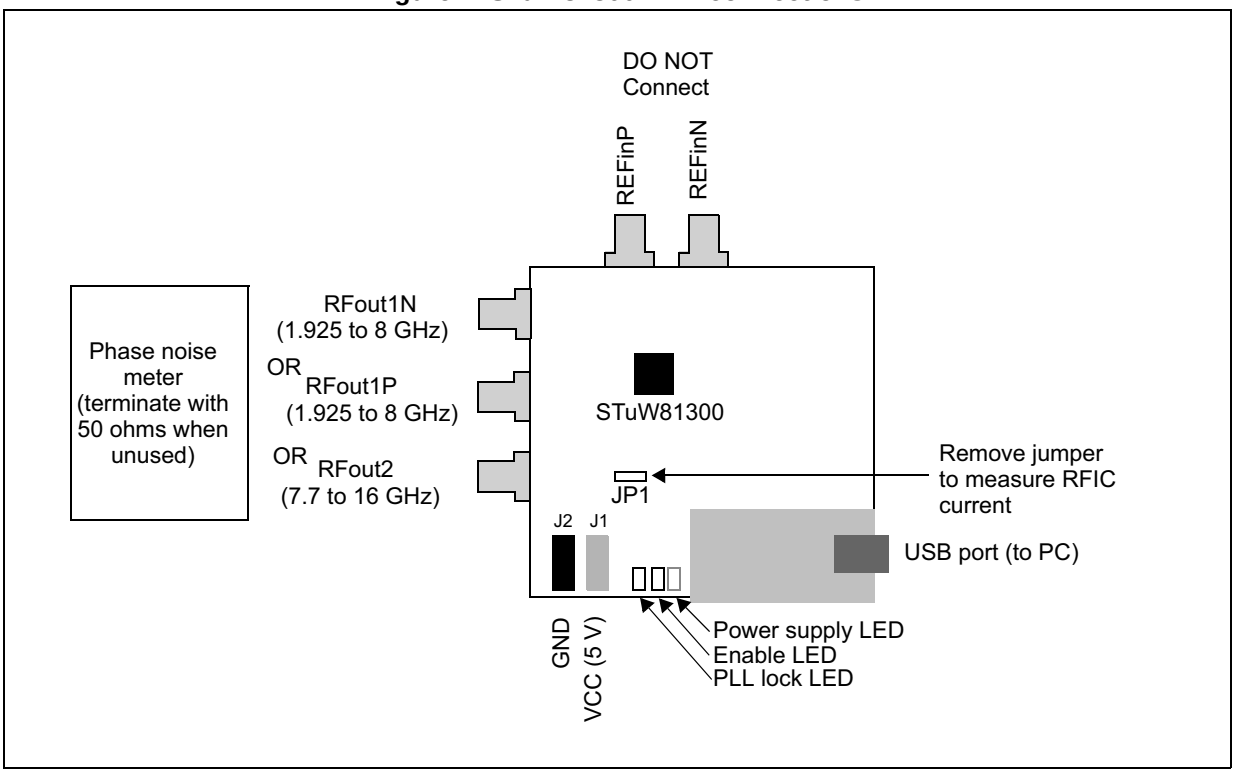
Figure 1. STuW81300-EVB connections



1.1 RF outputs

Connectors are provided for a phase-noise meter (or a spectrum analyzer) such as an Agilent E5052A/B (with E5053A microwave down-converter extension):

- RFout1N/P makes RF signal power directly available from the RF1 differential output port pins
- RFout2 makes RF signal power available through a PCB rat-race balun which combines the power of the RF2P/N pin outputs and delivers it to the SMA connector with optimized impedance matching across the RF2 frequency range.

Note: It is recommended to terminate unused port connectors with 50-ohm coaxial terminations.

1.2 Vcc

Power supply connection. USB power can be used instead of J1/J2 although this is not recommended. (Check the USB PC port current capability.)

1.3 USB (port B)

Provision for a USB cable connection to the PC running the STuW81300-EVB GUI.

1.4 LEDs

These are active only if the STuW81300-EVB GUI is running. From left to right:

- STuW81300 is in LOCK state (green). The same information is available in the STuW81300 EVAL GUI.
- STuW81300 is ENABLED (green).
- An unregulated 5 V supply is applied from the power connectors or USB port (red).

1.5 EXT VCO

This is not used in the default setup, however it is included to support the use of an external VCO when the characteristics required differ from those of the STuW81300 on-chip VCOs.

1.6 REFinP/N

This is not used in the default setup, however it is included to support the use of an external reference signal.

The STuW81300-EVB incorporates a low-noise CMOS 100 MHz reference crystal oscillator (not temperature compensated) and a 50 MHz crystal on the board underside which is not connected to the STuW81300 in the delivered board configuration, but which can be connected with some simple soldering operations. (Some component configurations are not connected to the STuW81300 in the delivered configuration.)

As the device supports different reference signal standards (CMOS, LVDS, LVECL) REFinP/N can be used to inject a reference signal from a low-noise synthesized signal generator. The REFin signal is critical for the phase noise and spur performance of the STuW81300.

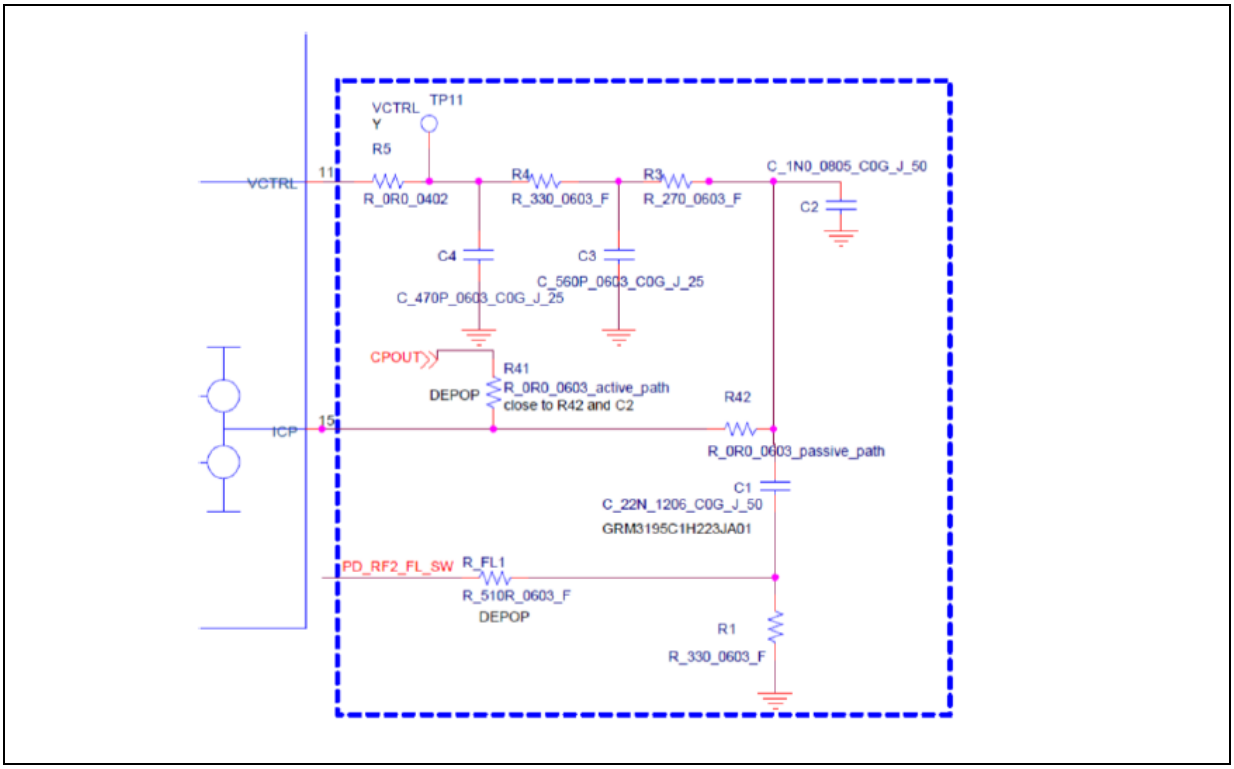
1.7 Enables/power down

Once the STuW81300-EVB is connected to a supply, the GPIO controls for the STuW81300 power-down, XTAL oscillator enable and RF1/2 output-stage power-downs are available through the STuW81300 EVAL GUI.

The only HW switch required is the single jumper (U5) that controls the power supply of the optional external VCO.

2 Loop filter

Figure 2. Loop filter schematics



Note: The VCO gain varies appreciably. Although not demonstrated in these instructions, the charge-pump current is automatically adjusted to partially account for variation due to VCO gain with loop control voltage. It can also be manually tuned versus VCO frequency.

Typically the loop filter and charge pump gain used are a good compromise between spur rejection and integrated phase-noise performance.

The loop filter is designed for the following nominal values: 60 kHz loop bandwidth, ~55° loop phase-margin, 3 mA charge-pump current and 50 MHz phase-frequency detector frequency.

3 STuW81300-EVB GUI setup

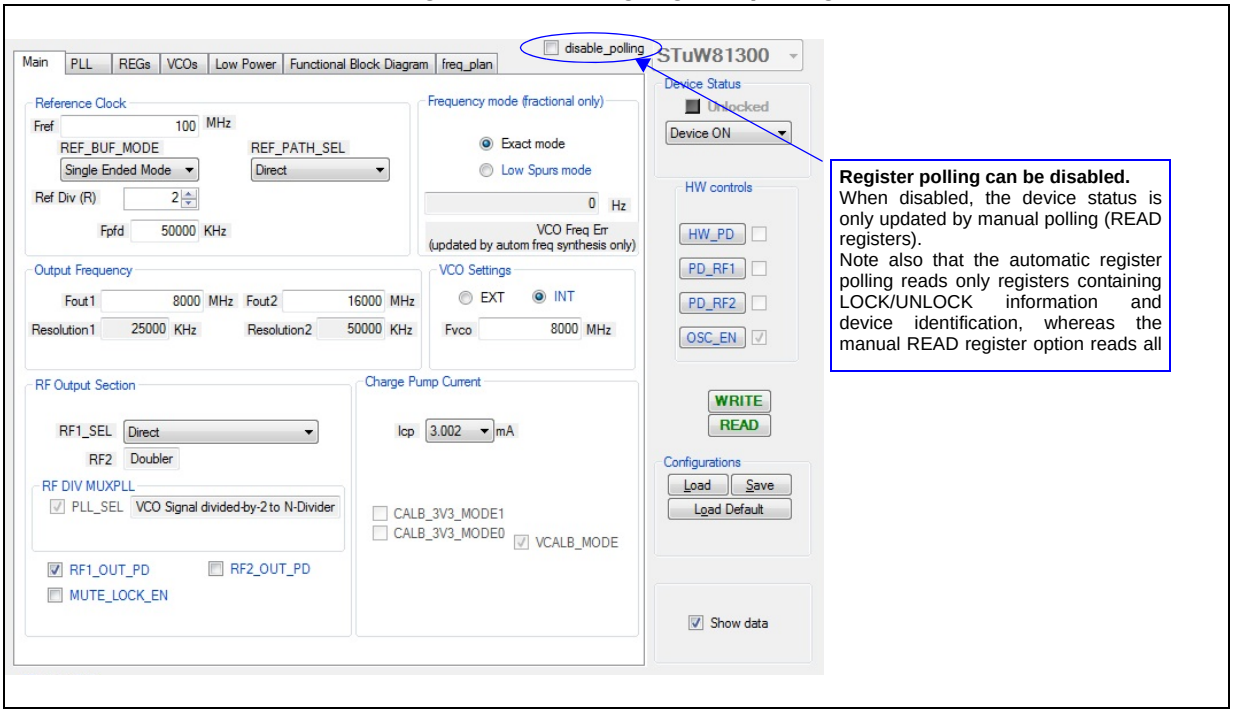
Before using the STuW81300-EVB the FTDI drivers must be installed. The following quick setup and power-on sequence can then be performed:

1. Supply the STuW81300-EVB power through J1/2.
2. Connect a USB cable from the PC to the STuW81300-EVB board.
3. Check that the USB device is properly recognized by the PC and that drivers are installed (CDM21206_Setup).
4. Start the GUI (STuW81300GUI.exe). The window shown in *Figure 5: STuW81300-EVB GUI window* should be displayed.
5. Check the GUI message list (USB Port is open, communication OK).
6. Configure all user settings (default, or load a previously defined configuration).
7. Click the WRITE button of the GUI to upload settings to the STuW81300 registers.

The USB communication is automatically established between the GUI and the STuW81300 when the GUI is started (see point 4 of GUI setup above). This ensures that if the STuW81300 is disconnected or its power supply is removed, the GUI detects this and gives a warning.

The user must close the GUI, restore hardware connections and re-open the GUI to re-establish the communication before being able to WRITE to the registers again. The USB communication (that is, register polling) can be disabled through the GUI as shown in *Figure 3*.

Figure 3. Disabling register polling



The GUI frequently uses the message list window to inform the user of any action being performed on the device, and to give a real-time aid-to-understanding of what is happening inside the STuW81300. We strongly suggest reading these messages.

For each of the objects present inside the GUI (buttons, text boxes, menus and so on) a brief description is available for a few seconds when the user passes the mouse cursor over the object. In this way the GUI passes detailed information to the user, minimizing the need for separate documentation.

Notes about RFIC current consumption measurement in the STuW81300-EVB

The STuW81300-EVB has 3 active parts on-board:

- USB module
- crystal oscillator
- STuW81300

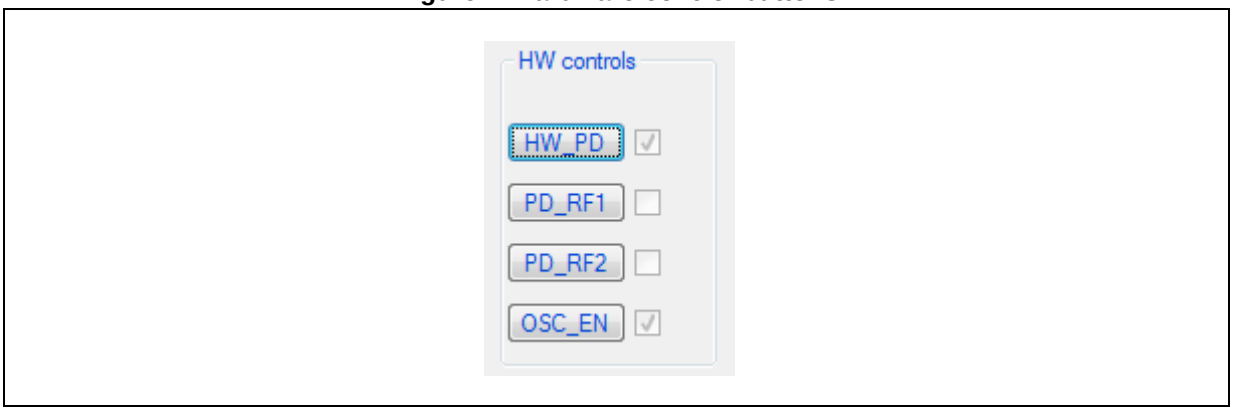
All the electronics is supplied through J1/J2 banana connectors (5 V) or through a USB cable (S1 in *Figure 15: STuW81300-EVB analog, RF and main signals*). Supplying power through a USB cable is not recommended for laboratory measurements, but it can be useful if the user needs to check the board functions in an office environment. The following points should also be noted:

- The crystal oscillator is not directly supplied through J1/J2 or the USB cable, but from the regulated voltage of the low-drop output voltage regulator integrated in the STuW81300, VREG_PLL (VREG_REF pin#19).
- The typical current measured through J1/J2 is the sum of the USB module (~80 mA), the STuW81300 and the crystal oscillator (~10 mA).
- To perform accurate current measurements on the STuW81300 crystal, current jumper JP1 can be used.

The correct procedure for accurate measurements of the RFIC current is as follows:

1. Insert an ammeter in the JP1 power line. Check that the voltage drop through JP1 is negligible.
2. Select STuW81300 HW_PD and OSC_EN (*Figure 4*). Current consumption is approximately 15 mA (5 mA STuW81300 + 10 mA crystal oscillator).
3. Disable OSC_EN and calculate the consumption of the crystal oscillator (IccOSC)
4. Program the STuW81300 in the required configuration and/or operating mode.
5. Measure the current through JP1 (IccOperating).
6. Calculate IccSTW = IccOperating - IccOSC.

Figure 4. Hardware control buttons

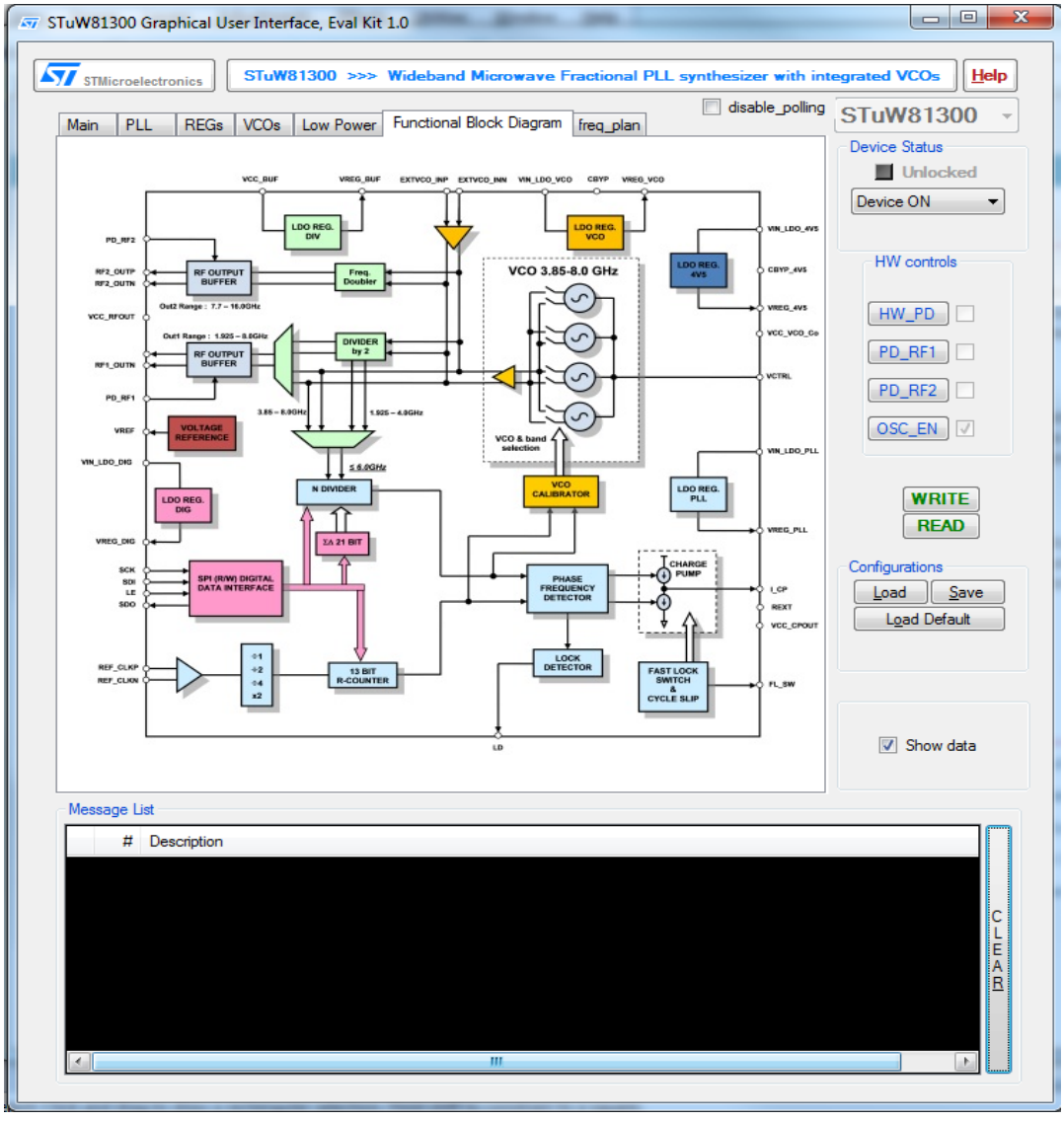


4 STuW81300-EVB GUI overview

The STuW81300-EVB GUI (STSW-RFSOL003) provides different tabs to set all available STuW81300 features as detailed in this section. The device status control can be used as an alternative to the HW_PD GPIO control to set the STuW81300 to ON or power down mode. If the board is ON, two on-board LEDs indicate the device status:

- the red LED indicates the supply is connected
- the green ENABLE LED indicates the device status is ON.

Figure 5. STuW81300-EVB GUI window



Note: The green LED can illuminate falsely when the USB module is not configured (that is, the GUI is not started), or when the GUI shows errors (provided that the register polling is not disabled) while the board is not under operating conditions.

Four hardware controls are available and are effective immediately (there is no need to perform a WRITE command):

- **HW_PD** sets the STuW81300 to power-down or active mode
- **PD_RF1/2** disable the RF outputs
- **OSC_EN** acts on the on-board oscillator standby pin.

Two buttons are available to **WRITE** or **READ** all STuW81300 registers.

GUI configurations can be saved or loaded through the following buttons:

- **Load**: loads previously saved configuration from a file
- **Save**: saves the current configuration to a file
- **Load Default**: restores the default configuration.

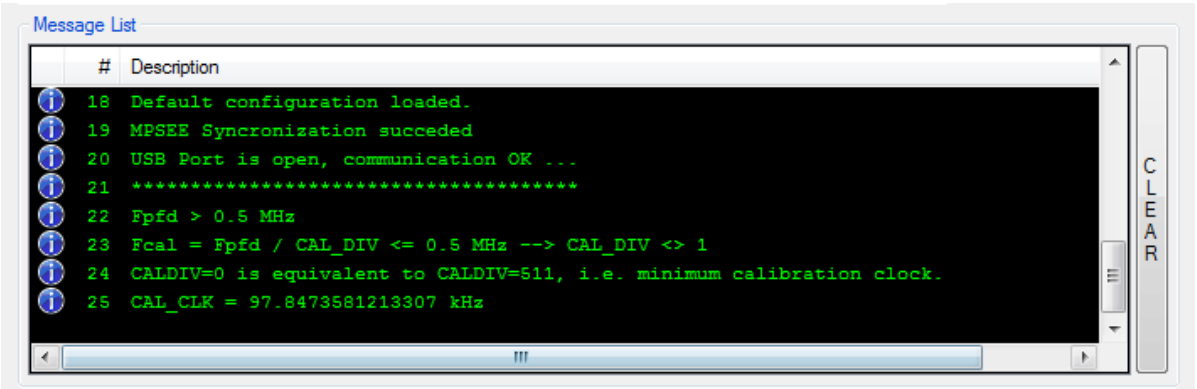
The user can show/hide register content (after a WRITE/READ command) in the Message List window using the **Show Data** check button.

The **message list** is a powerful instrument that supports the user during normal operation of the GUI. It gives useful information about:

- FTDI communication information
- STuW81300 ID
- Registers R/W
- Lock detection
- VCO/Word selected by calibrator or user
- Regulators ready/over current detection.

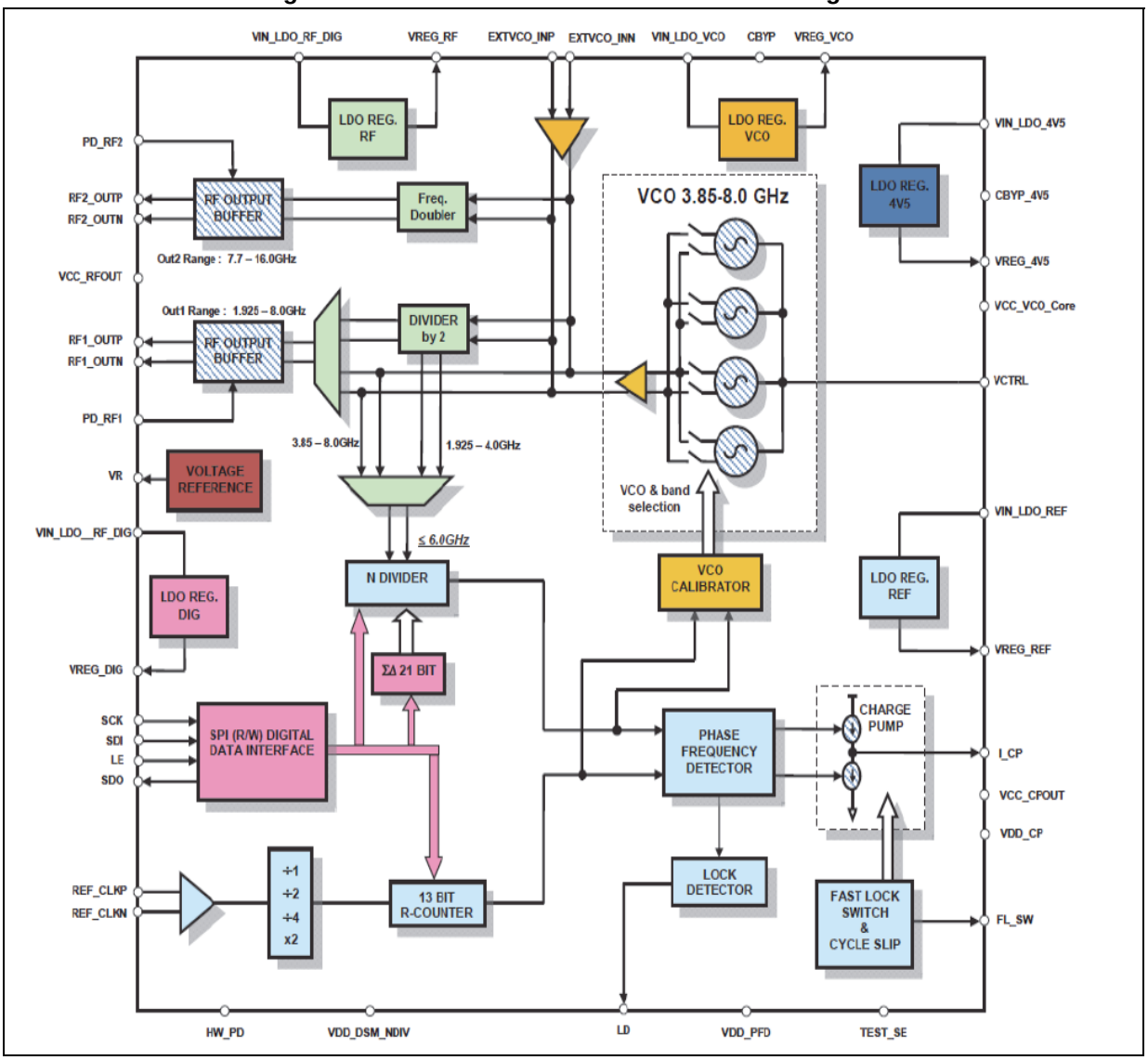
The GUI always checks the SWT81300 lock and ID (poll time = 1s). This feature is provided so that any unintentional USB cable disconnect or other incorrect user intervention is reported and the user can correct the issue.

Figure 6. Message output example



For quick reference the circuit block diagram is given in *Figure 7*. Reading the STuW81300 data sheet *[1]* is recommended for a detailed understanding of all circuit features, blocks and registers.

Figure 7. STuW81300-EVB functional block diagram



5 STuW81300-EVB GUI programming tabs

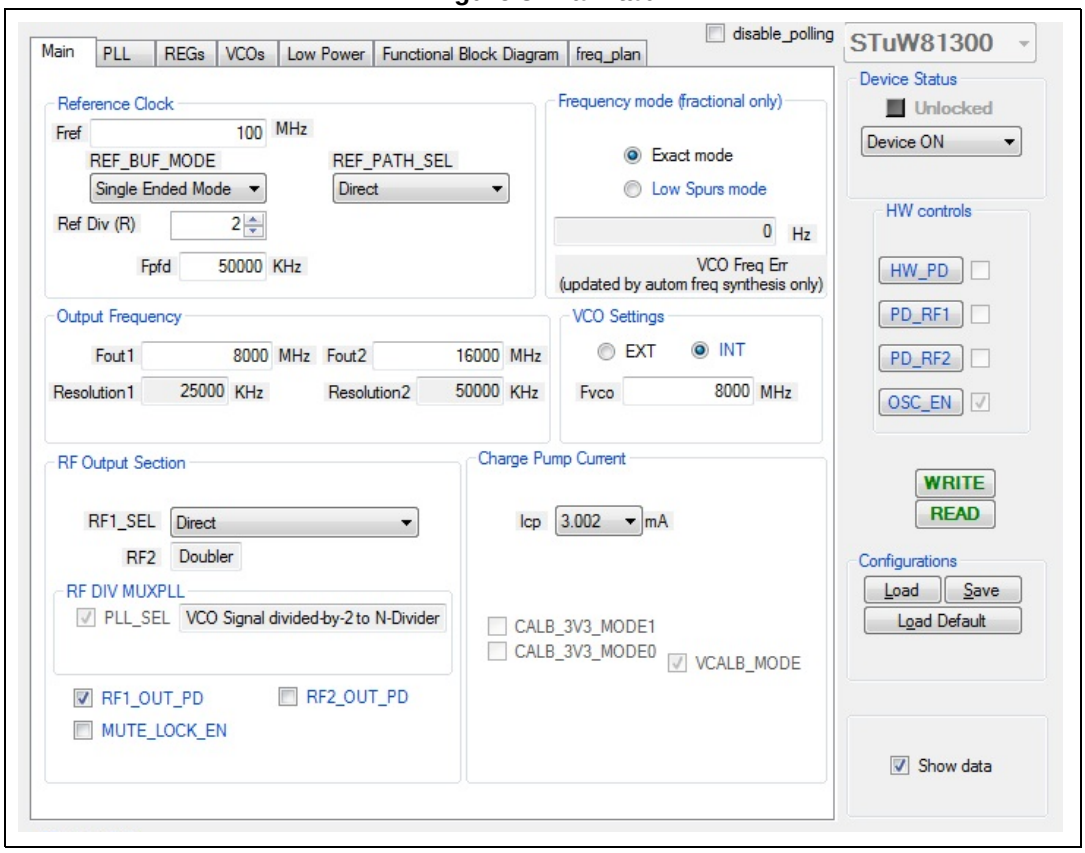
Six tabs are available to control the different parts and user modes of the STuW81300.

- *Section 5.1: Main tab*
- *Section 5.2: PLL programming tab*
- *Section 5.3: Regulator programming tab*
- *Section 5.4: VCO programming tab*
- *Section 5.5: Low-power programming tab*.
- *Section 5.6: Freq_plan tab*

5.1 Main tab

The **Main** tab (*Figure 8*) groups all the commonly used controls and resulting information required for basic use of the STuW81300.

Figure 8. Main tab



The Main tab is divided in six main sections detailed below.

5.1.1 Frequency mode (fractional only)

The user can select between two synthesizer operating modes. Although in most of the configurations the differences are negligible, in some cases mode selection can be useful:

Frequency modes (exact or low spur) are enabled only if the fractional divider is used (N_{INT} < 508).

- **Exact mode**: due to the flexible architecture of the delta sigma modulator embedded in STuW81300, the synthesized frequency is **exactly** the frequency requested by user.
- **Low Spurs mode**: in this mode there is an improvement on spur signals at the expense of a slight frequency error. The error is less than half resolution and it is indicated in the Freq Err value. Under typical operating conditions the error is < 0.01 ppm.

5.1.2 Reference clock

The user must enter the reference frequency (either from an external source or crystal oscillator), reference divider ratio or PFD frequency.

The relationship Fref=R*F_{PFD} is always guaranteed by the GUI.

5.1.3 Output frequency

Output frequency indication of RF1 and RF2 (the available resolution depends on whether exact or low-spurs mode is used).

The user can enter the RF1 output frequency or VCO frequency directly. The RF2 output frequency is calculated by doubling the VCO frequency.

Resolution1/2 are read-only fields. Their values depend on the F_{PFD} and the frequency synthesis (integer/fractional). With respect to the VCO resolution (not shown) it should be noted that:

- the RF1 resolution is affected by RF1_SEL (division by 1 or by 2)
- the RF2 resolution is affected by the doubler fixed ratio (multiplication by 2).

See *Figure 9: PLL programming tab*.

5.1.4 VCO settings

The user must consider the following points when applying settings to the VCO:

- The choice between enabling internal VCOs, or an external VCO if mounted on the EVAL board. Alternatively some rework can be done to the STuW81300-EVB board to allow an external VCO signal to be fed through J17.
- The internal VCO frequency can be programmed, or the external VCO option can be used. The VCO frequency can be entered for both options (internal or external VCO).
- The allowed range for internal-VCO oscillation frequency values is 3850 MHz to 8000 MHz.
- The user can enter the VCO frequency, in which case the RF1 output frequency is calculated according to RF1_SEL, while the RF2 output frequency is always twice the VCO frequency.

5.1.5 RF output section

The user can apply the following settings to the RF output section:

- RF1_SEL (VCO signal direct to the RF1 output, or through divider-by-two)
- RF1 or RF2 output stage power-downs (independently).

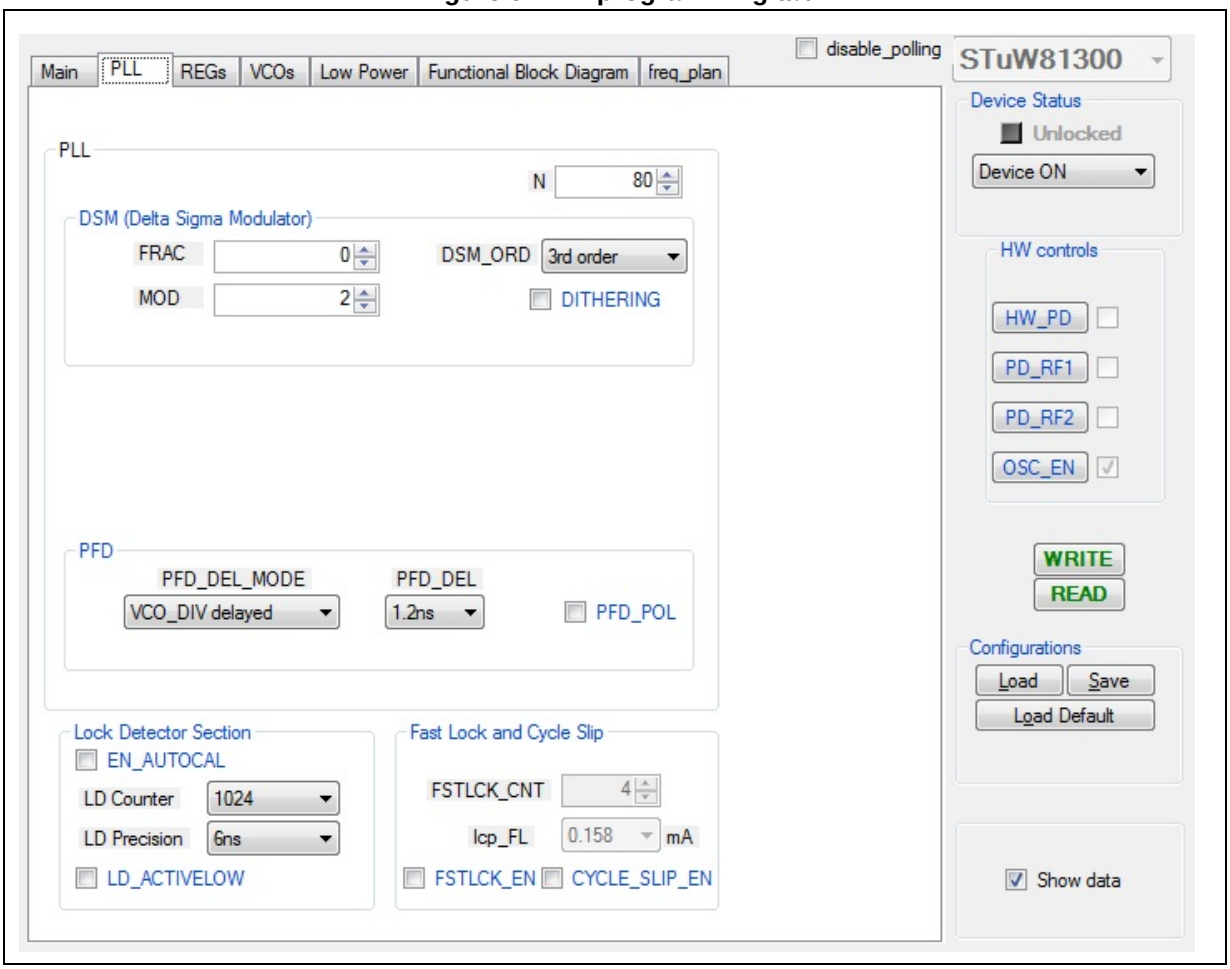
5.1.6 Charge pump current

The user can set the nominal charge pump current (Icp) to control loop parameters (bandwidth and phase margin).

5.2 PLL programming tab

This section details the **PLL settings** tab shown in (*Figure 9*).

Figure 9. PLL programming tab



The PLL tab shows the advanced functions of the STuW81300.

Most of the PLL-section settings (FRAC, MOD, N, DITHERING) within the PLL tab are automatically calculated through an algorithm which starts when the input frequency is set by the user. All the other frequencies in the Main tab are updated accordingly. Alternatively, the user can set the desired FRAC, MOD and N settings directly (this does not start the algorithm).

Unlike the FRAC, MOD and N settings, applying the DITHERING setting starts the algorithm.

Note: The user has direct access to the DITHERING setting in EXACT MODE only

Before changing these parameters, it is recommended to refer to the STuW81300 datasheet *[1]*, in particular regarding the DSM settings, as this can affect the performance.

The PLL tab is divided into three sections:

- PLL section
  - N setting
  - DSM group settings: FRAC, MOD, DITHERING, DSM order
  - PFD group settings: PFD anti-backlash delay and delay mode, PFD polarity.
- Lock Detector section

  The Lock detector counter and precision tune the lock detection mechanism in order to correctly acknowledge the PLL-lock condition. The lock acknowledgment is based on lock-condition stability for a minimum number of PFD cycles (that is, the counter value must be high enough) and with the lowest delay between the UP and DOWN output signals (low values equate to highest precision). When the user sets the LD_ACTIVELOW check box, the polarity of the lock detector pin changes. The following conditions apply:
  - LD_ACTIVELOW checked:

    PLL LOCK -> lock detector pin=GND

    PLL UNLOCK -> lock detector pin=VDD
  - LD_ACTIVELOW unchecked:

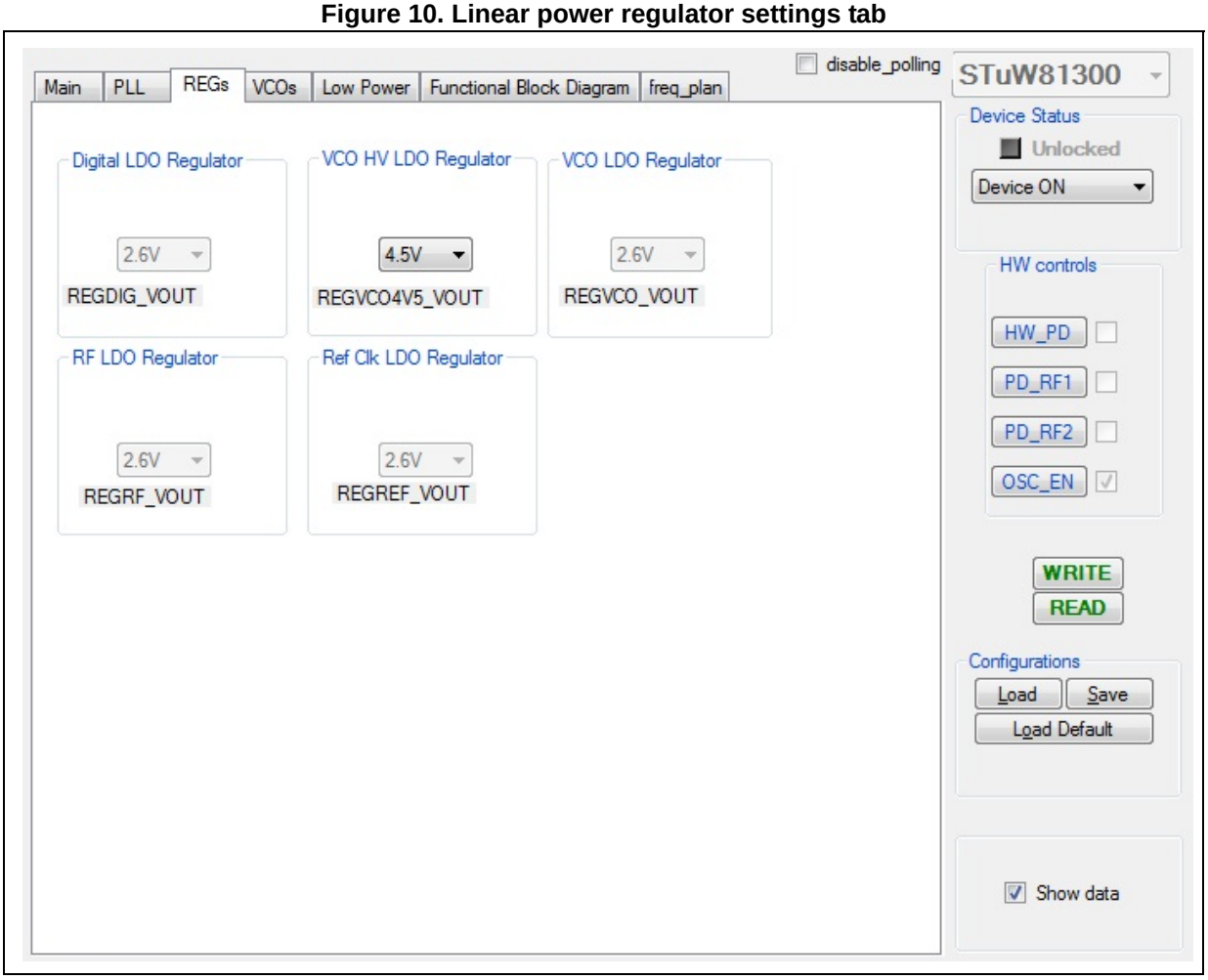
    PLL LOCK -> lock detector pin=VDD

    PLL UNLOCK -> lock detector pin=GND
  - The GUI and the EVAL Board Lock LED are not affected by the polarity settings since the GUI sets them taking into account the LD_ACTIVELOW status, thus showing the lock condition independently of LD_ACTIVELOW
- Fast Lock and Cycle Slip section
  - Enable and set Fast lock or cycle slip functionality, see the STuW81300 datasheet *[1]* for details.

5.3 Regulator programming tab

This section details the linear regulator settings tab (**REGs)** shown in *Figure 10*. (The voltages shown are for illustrative purposes only.)

Figure 10. Linear power regulator settings tab

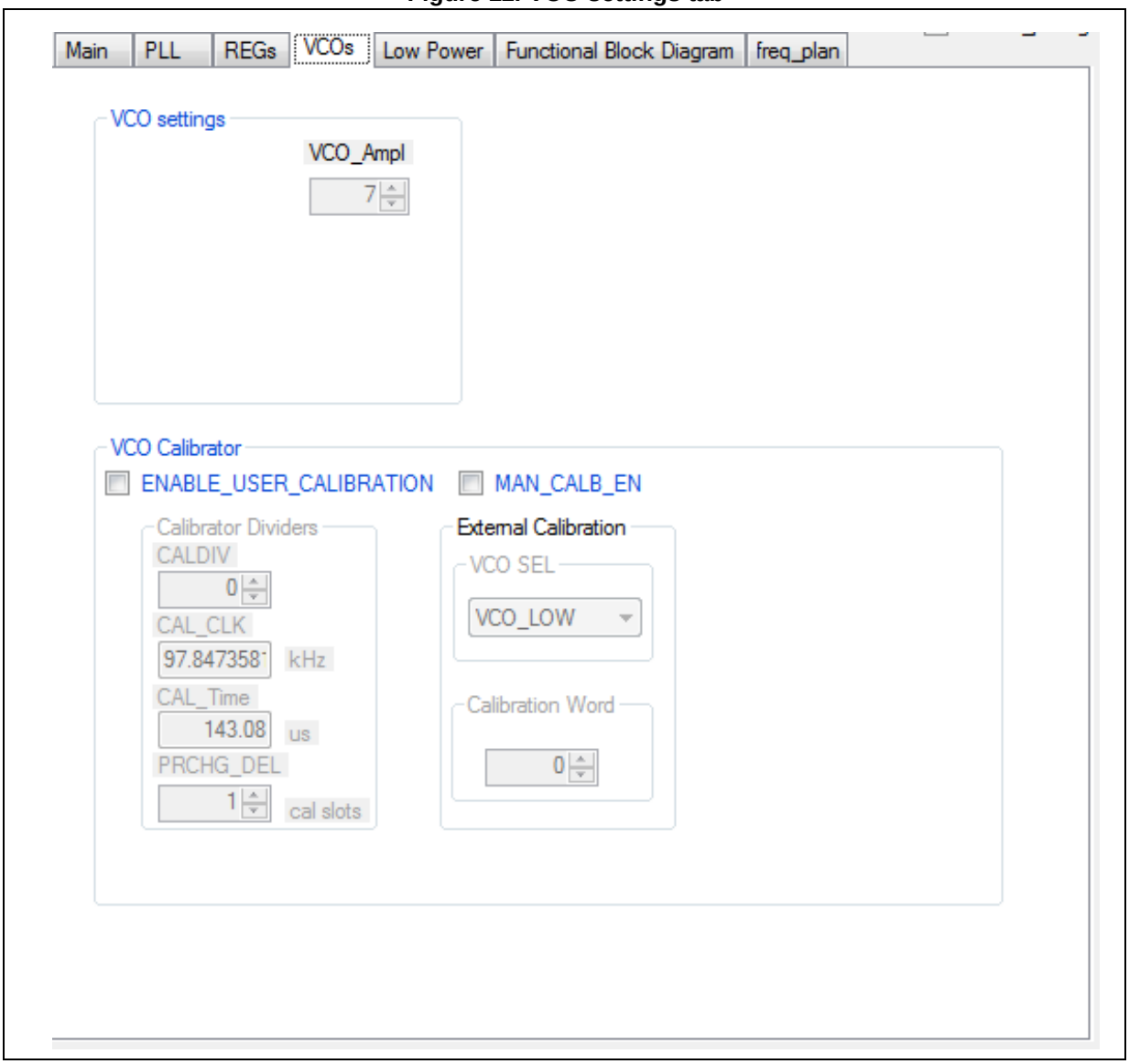


The STuW81300 embeds 5 LDOs in order to achieve optimal supply noise rejection and IC-block decoupling.

5.4 VCO programming tab

This section details the VCO settings tab shown in *Figure 11*.

Figure 11. VCO settings tab



The tab is divided in two main sections:

- **VCO settings**: the VCO_Ampl value is shown here for information purposes only.
- **VCO Calibrator**
  The user can initiate a calibration with associated parameters CALDIV and PRCHG_DEL. The calibration clock frequency (CAL_CLK) is derived by dividing the PFD frequency by CALDIV. The pre-charge delay can be used to obtain more accurate results. The calibration time is also displayed. The calculations deriving these numbers are visible by holding the mouse over each item.

  The STuW81300 has four integrated VCOs, each with 32 sub-bands (VCO_WORDs). The selection of a sub-band is done in either of the following operating modes:

  – **Automatic selection** *(default calibration)*.

    The user enters the required frequency and performs a register WRITE. The device then runs an internal calibration algorithm, with calibration time displayed in the CAL_Time field. The algorithm finds the most appropriate VCO/VCO_WORD combination and so synthesizes the frequency. The reference signal is needed to perform a calibration.

  – **Manual selection** of VCO/VCO_WORD combination (external calibration).

    In this case *the calibration circuit is disabled* and the VCO/VCO_WORD combination can be programmed immediately without the need to wait for the CAL_Time to elapse. This feature is useful in fast frequency-hopping applications, as it allows the user to reuse previously stored VCO/VCO_WORD register settings.
    A previous default calibration of a single or a multiple set of frequencies for each channel is needed in order to store the VCO/VCO_WORD combinations, which are readable through SPI registers. External calibration is enabled by the MAN_CALB_EN check box that disables the internal (default) calibration procedure and allows the VCO and WORD settings to be forced. The overall settling time for a frequency change is thus reduced as the STuW81300 does not run the calibrator.

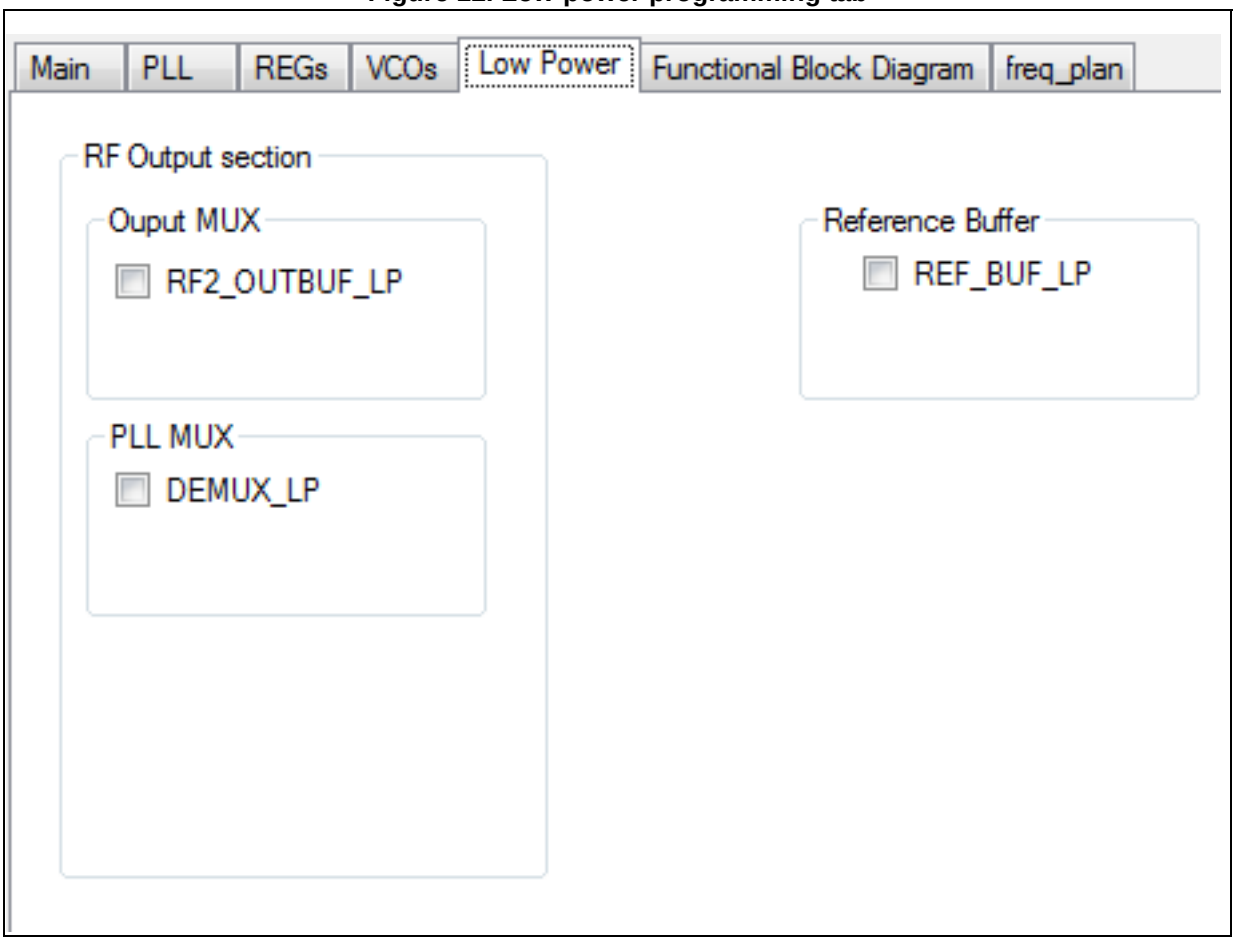
  The overall settling time has to be minimized. The manual selection method effectively reduces the time to synthesize a frequency, given a batch of previous calibrations. Another possibility is to use the double buffering of the registers in the default calibration mode. The affected registers are those directly related to the frequency synthesis (ST3-ST2-ST1 content is buffered and sent along with the ST0 content, not earlier). See the STuW81300 datasheet *[1]* for details.

Note: The GUI uses double buffering by default.

5.5 Low-power programming tab

This section details the low-power programming tab shown in *Figure 12*.

Figure 12. Low-power programming tab



This TAB allows the user to apply low-power mode to respective circuit sections. It allows the user to balance overall current consumption against performance.

Note: Not all circuit sections are always on (for example if RF2 is off, then RF2_OUTBUF_LP has no effect).

5.6 Freq_plan tab

This section details the freq_plan programming tab shown in *Figure 13*.

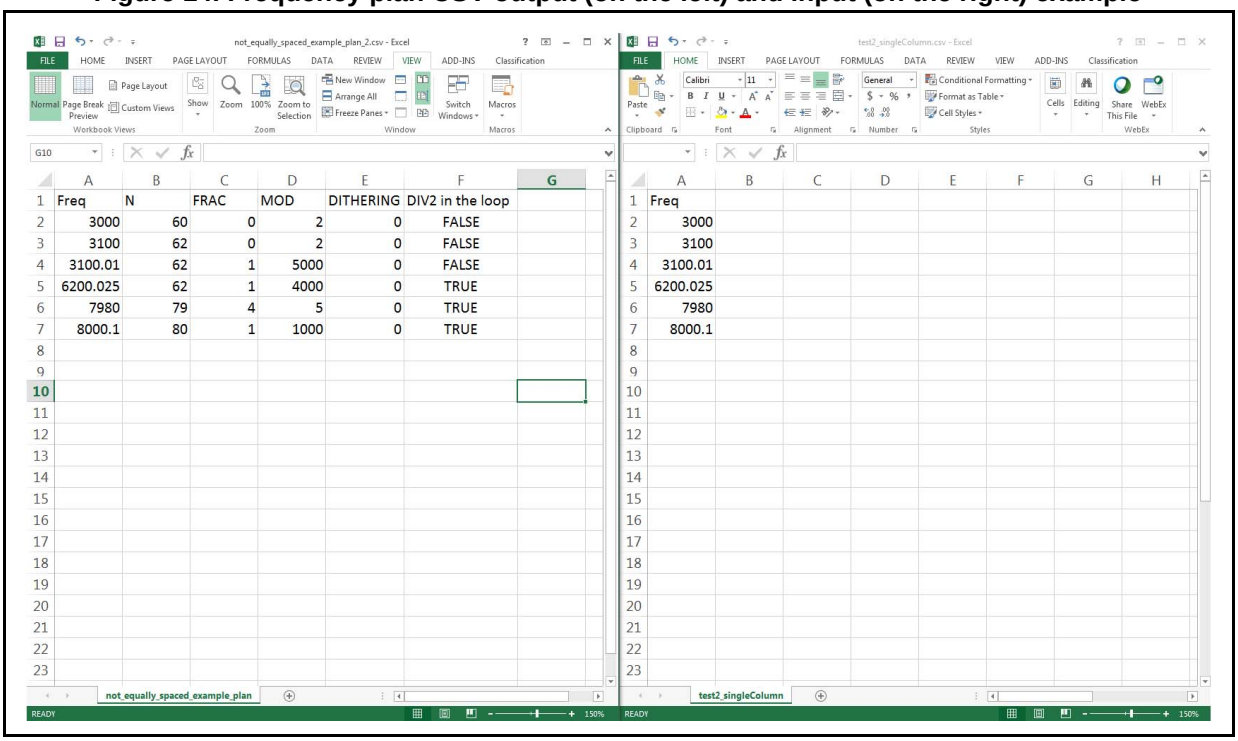
Figure 13. Freq_plan programming tab

A VCO **frequency plan** can be generated and stored in a *.csv* file using either of the methods proposed. This *programming* plan provides each VCO frequency with settings corresponding to the required synthesis, that is the: N, FRAC, MOD, DITHERING settings. These settings depend on parameters from the other TABs (F_{PFD}, frequency mode and so on).

Note: The algorithm also works for frequencies outside the VCO nominal frequency range (see example in Figure 14).

1. Based on Fstart, Fstop and Fstep inputs (in MHz), the algorithm generates a programming plan with equally spaced frequency points. The plan is stored to a .csv file, the name and path of which can be defined by the user, using the normal windows dialog box. The number of frequency points is also given as an output in a dedicated field of this GUI tab.
2. Based on a .csv file listing of the frequencies we wish to synthesize (see example in *Figure 14*), the algorithm generates a programming plan to a new .csv file showing the settings for synthesis of each desired frequency.

Figure 14. Frequency plan CSV output (on the left) and input (on the right) example

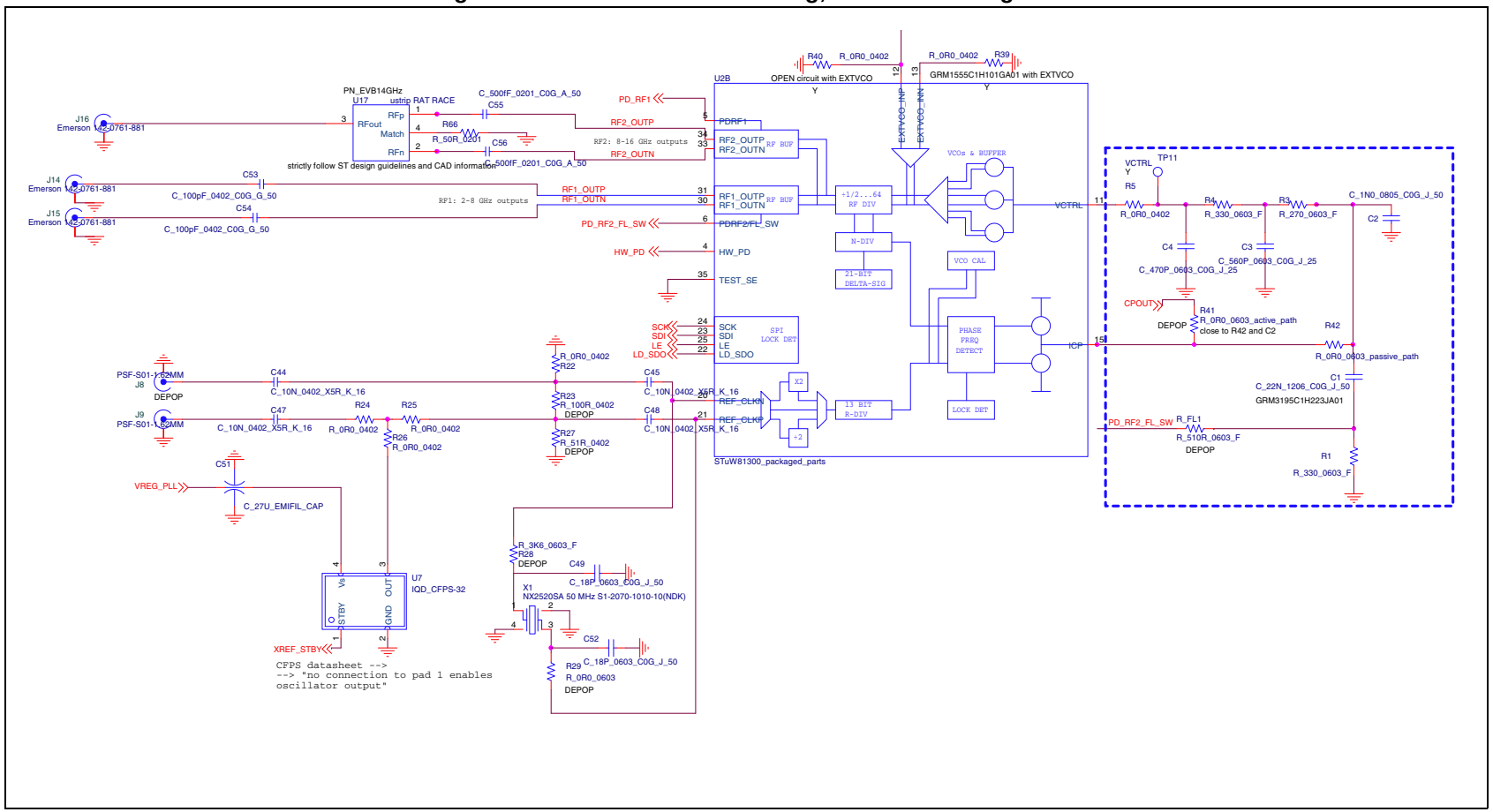


Freq	N	FRAC	MOD	DITHERING	DIV2 in the loop
3000	60	0	2	0	FALSE
3100	62	0	2	0	FALSE
3100.01	62	1	5000	0	FALSE
6200.025	62	1	4000	0	TRUE
7980	79	4	5	0	TRUE
8000.1	80	1	1000	0	TRUE

Freq
3000
3100
3100.01
6200.025
7980
8000.1

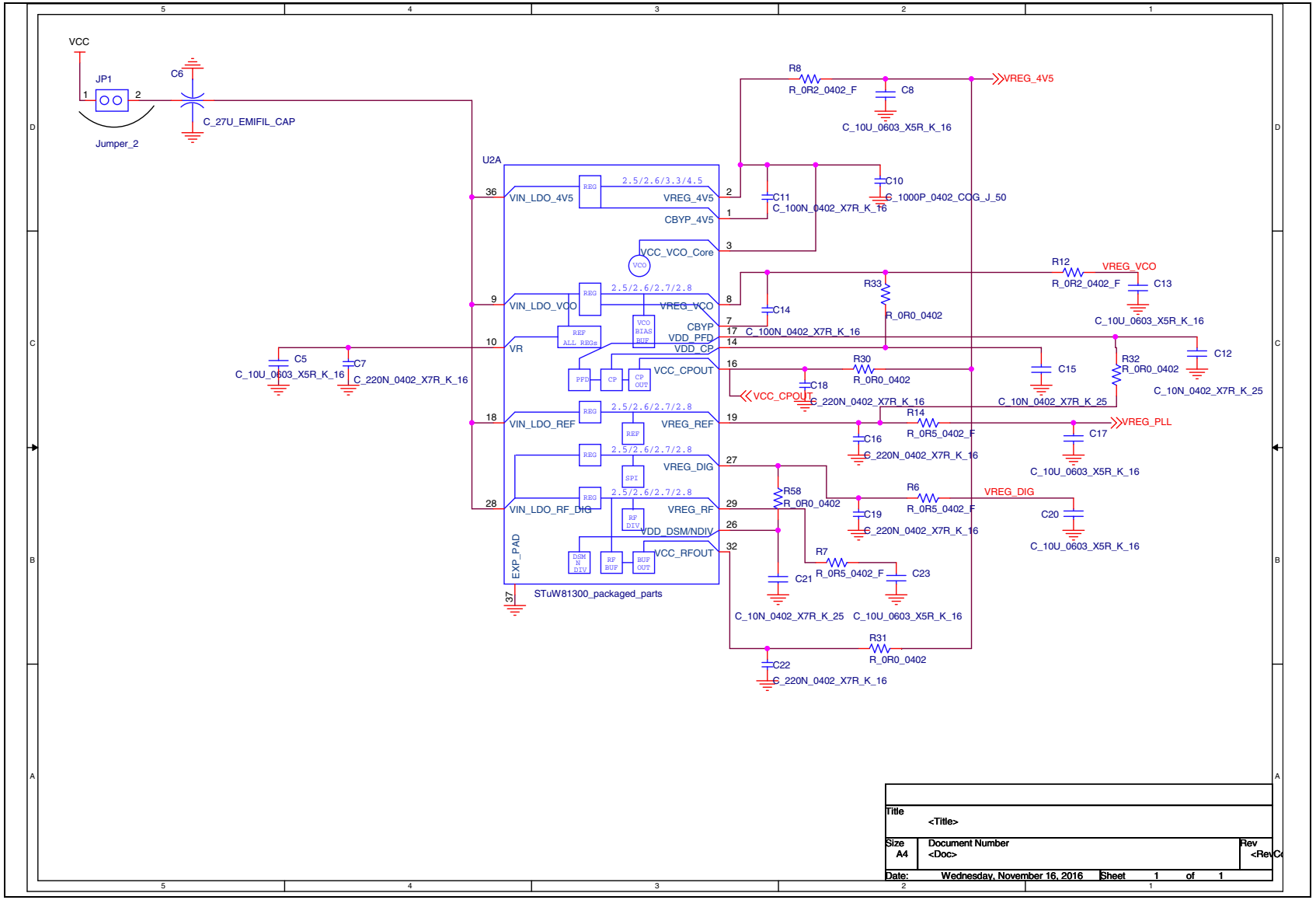
6 STuW81300-EVB schematics

Figure 15. STuW81300-EVB analog, RF and main signals



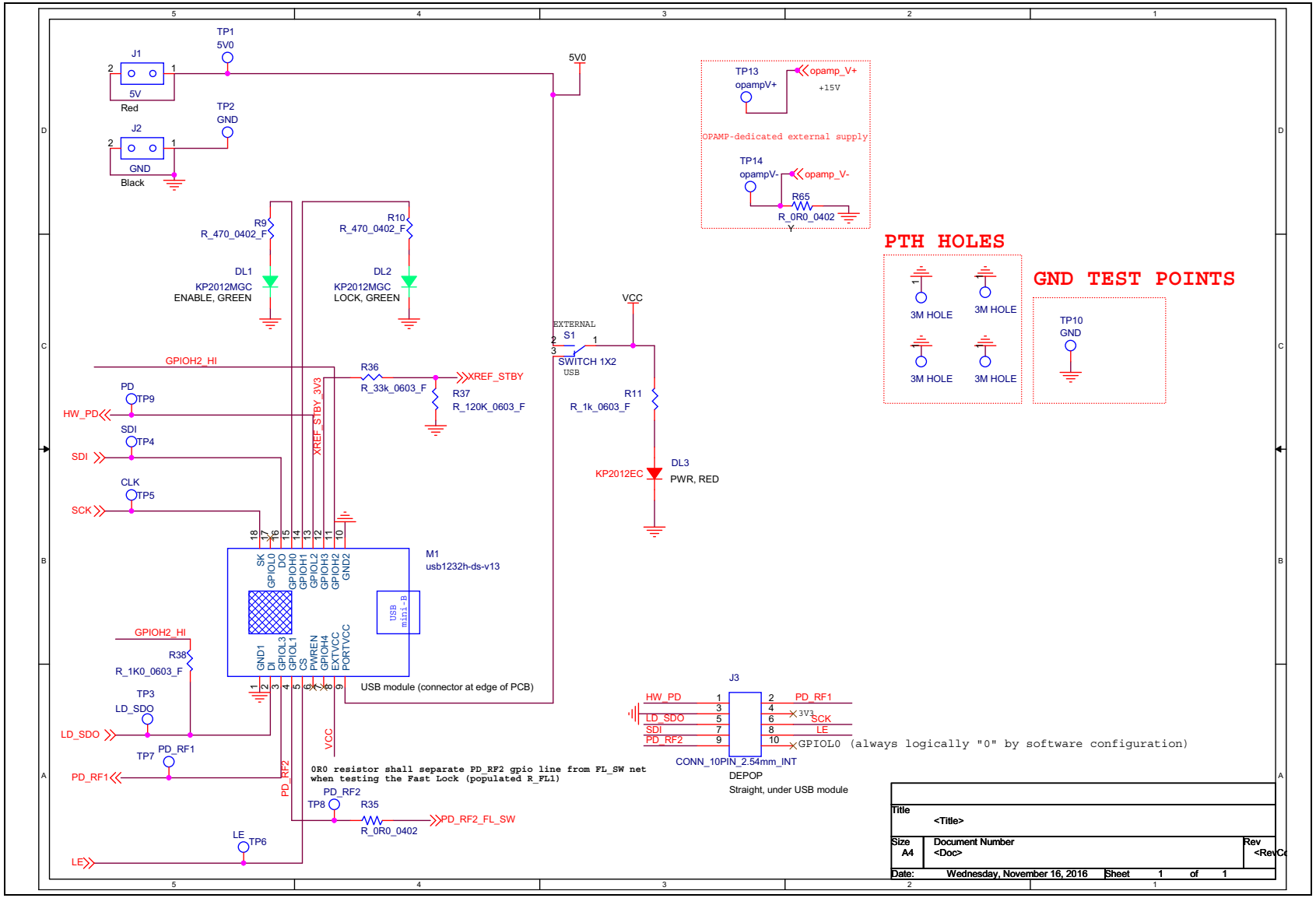
Note: Updated part values and part numbers are given in Section 7: STuW81300-EVB BOM.

Figure 16. STuW81300-EVB power supply



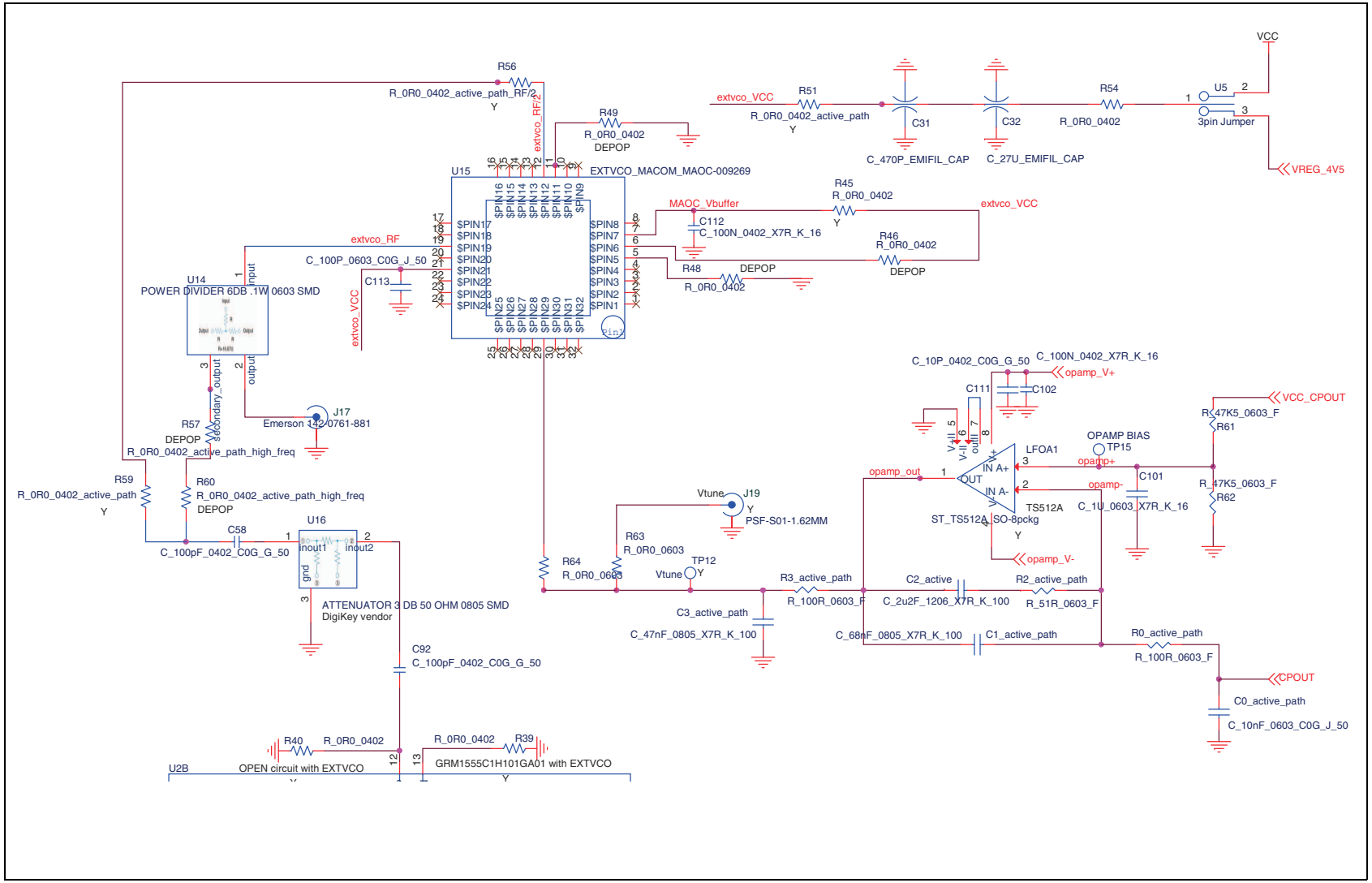
Note: Updated part values and part numbers are given in Section 7: STuW81300-EVB BOM.

Figure 17. STuW81300-EVB interface



Note: Updated part values and part numbers are given in Section 7: STuW81300-EVB BOM.

Figure 18. STuW81300-EVB more analog, RF and optional signals



Note: Updated part values and part numbers are given in Section 7: STuW81300-EVB BOM.

7 STuW81300-EVB BOM

Table 1. STuW81300-EVAL BOM v2.0

Reference	Value	Manufacturer	Part Number	Populated
C0_active_path	C_10nF_0603_C0G_J_50	Murata	GRM1885C1H103JA01	Y
C1	C_22N_1206_C0G_J_50	Murata	GRM3195C1H223JA01	Y
C1_active_path	C_68nF_0805_X7R_K_100	Murata	GRM21BR72A683KAC4	Y
C2_active	C_2u2F_1206_X7R_K_100	Murata	GRM31CR72A225KA73	Y
C2	C_1N0_0805_C0G_J_50	Murata	GRM2165C1H102JA01	Y
C3_active_path	C_47nF_0805_X7R_K_100	Murata	GRM21BR72A473KA01	Y
C3	C_560P_0603_C0G_J_25	Murata	GRM1885C1H561JA01	Y
C4	C_470P_0603_C0G_J_25	Murata	GRM1885C1H471JA01	Y
C5,C13,C20, C23	C_10U_0603_X5R_K_16	Murata	GRM188R61C106MA73	Y
C6,C32,C51	C_27U_EMIFIL_CAP	Murata	NFM31PC276B0J3	Y
C7,C16,C18, C19, C22	C_220N_0402_X7R_K_16	Murata	GRM155R71C224KA12	Y
C8,C17	C_10U_0603_X5R_K_16	Murata	GRM188R61C106MA73	Y
C10	C_1000P_0402_COG_J_50	Murata	GRM1555C1H102JA01	Y
C11,C14	C_100N_0402_X7R_K_16	Murata	GRM155R71C104KA88	Y
C12	C_10N_0402_X7R_K_25	Murata	GRM155R71E103KA01	Y
C15,C21	C_10N_0402_X7R_K_25	Murata	GRM155R71E103KA01	Y
C31	C_470P_EMIFIL_CAP	Murata	NFM18CC471R1C3	Y
C44,C45,C47, C48	C_10N_0402_X5R_K_16	Murata	GRM155R61C103KA01	Y
C49,C52	C_18P_0603_C0G_J_50	Murata	GRM1885C1H180JA01	Y
C53,C54,C92	C_100pF_0402_C0G_G_50	Murata	GRM1555C1H101GA01	Y

Table 1. STuW81300-EVAL BOM v2.0 (continued)

Reference	Value	Manufacturer	Part Number	Populated
C55,C56	C_500fF_0201_C0G_A_50	Murata	GRM0335C1HR50WA01	Y
C58	C_100pF_0402_C0G_G_50	Murata	GRM1555C1H101GA01	Y
C101	C_1U_0603_X7R_K_16	Murata	GRM188R71C105KA12	Y
C102	C_100N_0402_X7R_K_16	Murata	GRM155R71C104KA88	Y
C111	C_10P_0402_C0G_G_50	Murata	GRM1555C1H100GA01	Y
C112	C_100N_0402_X7R_K_16	Murata	GRM155R71C104KA88	Y
C113	C_100P_0603_C0G_J_50	Murata	GRM1885C1H101JA01	Y
DL1	KP2012MGC	Kingbright	KP2012MGC	Y
DL2	KP2012MGC	Kingbright	KP2012MGC	Y
DL3	KP2012EC	Kingbright	KP2012EC	Y
JP1	Jumper_2	Samtec	HTSW-102-07-G-S	Y
J1	5V	Emerson Network Power Connectivity Solutions	105-0752-001	Y
J2	GND	Emerson Network Power Connectivity Solutions	105-0753-001	Y
J3	CONN_10PIN_2.54mm_INT	TE Connectivity	2-176 1603-3	DEPOP(1)
J8	PSF-S01-1.62MM	Gigalane	PSF-S01-1.62MM	DEPOP(1)
J9	PSF-S01-1.62MM	Gigalane	PSF-S01-1.62MM	Y
J14,J15,J16,J17	Emerson 142-0761-881	Emerson Network Power	142-0761-881	Y
J19	PSF-S01-1.62MM	Gigalane	PSF-S01-1.62MM	Y
LFOA1	ST_TS512A_SO-8pckg	STMicroelectronics	TS512A	Y
MF1,MF2,MF3, MF4	3M HOLE	Keystone	25510	Y
M1	usb1232h-ds-v13	DLP design	USB1232H-ds-v13	Y
R_FL1	R_510R_0603_F	Yageo	RC0603FR-07510RL	DEPOP(1)
R0_active_path	R_100R_0603_F	Yageo	RC0603FR-07100RL	Y
R1,R4	R_330_0603_F	Yageo	RC0603FR-07330RL	Y
R2_active_path	R_51R_0603_F	Yageo	RC0603FR-0751RL	Y
R3	R_270_0603_F	Yageo	RC0603FR-07270RL	Y

Table 1. STuW81300-EVAL BOM v2.0 (continued)

Reference	Value	Manufacturer	Part Number	Populated
R3_active_path	R_100R_0603_F	Yageo	RC0603FR-07100RL	Y
R5,R22,R24,R25,R26,R30,R32,R33,R35,R45,R54,R58,R65	R_0R0_0402	Panasonic	ERJ-2GE0R00X	Y
R6,R7,R14	R_0R5_0402_F	Yageo	RL0402FR-070R5L	Y
R8,R12	R_0R2_0402_F	Yageo	RL0402FR-070R2L	Y
R9,R10	R_470_0402_F	Yageo	RC0402FR-07470RL	Y
R11	R_1k_0603_F	Yageo	RC0603FR-071KL	Y
R23	R_100R_0402	Panasonic	RC0402FR-07100RL	DEPOP(1)
R27	R_51R_0402	Panasonic	RC0402FR-0751RL	DEPOP(1)
R28	R_3K6_0603_F	Yageo	RC0603FR-073K6L	DEPOP(1)
R29	R_0R0_0603	Panasonic	ERJ-3GEY0R00V	DEPOP(1)
R31	R_0R0_0402	Panasonic	ERJ-2GE0R00X	Y
R36	R_33k_0603_F	Yageo	RC0603FR-0733KL	Y
R37	R_120K_0603_F	Yageo	RC0603FR-07120KL	Y
R38	R_1K0_0603_F	Yageo	RC0603FR-071KL	Y
R39	R_0R0_0402	Panasonic	ERJ-2GE0R00X	Y
R40	R_0R0_0402	Panasonic	ERJ-2GE0R00X	Y
R41	R_0R0_0603_active_path	Panasonic	ERJ-3GEY0R00V	DEPOP(1)
R42	R_0R0_0603_passive_path	Panasonic	ERJ-3GEY0R00V	Y
R46,R48,R49	R_0R0_0402	Panasonic	ERJ-2GE0R00X	DEPOP(1)
R51	R_0R0_0402_active_path	Panasonic	ERJ-2GE0R00X	Y
R56	R_0R0_0402_active_path_RF/2	Panasonic	ERJ-2GE0R00X	Y
R57,R60	R_0R0_0402_active_path_high_freq	Panasonic	ERJ-2GE0R00X	DEPOP(1)
R59	R_0R0_0402_active_path	Panasonic	ERJ-2GE0R00X	Y
R61,R62	R_47K5_0603_F	Yageo	RC0603FR-0747K5L	Y
R63,R64	R_0R0_0603	Panasonic	ERJ-3GEY0R00V	Y
R66	R_50R_0201	Panasonic	ERJ1GNYJ50RC	Y
S1	SWITCH 1X2	EOZ	09.03201.02	Y
TP1	5V0	Keystone	5005	Y
TP2,TP10	GND	Keystone	5006	Y
TP3	LD_SDO	Keystone	5007	Y
TP4	SDI	Keystone	5007	Y
TP5	CLK	Keystone	5007	Y
TP6	LE	Keystone	5007	Y

Table 1. STuW81300-EVAL BOM v2.0 (continued)

Reference	Value	Manufacturer	Part Number	Populated
TP7	PD_RF1	Keystone	5008	Y
TP8	PD_RF2	Keystone	5008	Y
TP9	PD	Keystone	5008	Y
TP11	VCTRL	Keystone	5005	Y
TP12	Vtune	Keystone	5005	Y
TP13	opampV+	Keystone	5005	Y
TP14	opampV-	Keystone	5006	Y
TP15	OPAMP BIAS	Keystone	5005	Y
U2	STuW81300	STMicroelectronics	STuW81300	Y
U5	3pin Jumper	Samtec	PHT-103-01-L-S	Y
U7	IQD_CFPS-32	IQD	LFSPXO056090	Y
U14	POWER DIVIDER 6DB .1W 0603 SMD	SUSUMU	PS1608GT2-R50-T5	Y
U15	EXTVCO_MACOM_MAOC-009269	MA-COM	MAOC-009269	DEPOP(1)
U16	ATTENUATOR 3 DB 50 OHM 0805 SMD	SUSUMU	PAT1220-C-3DB-T5	Y
U17	ustrip RAT RACE	(printed balun)	PN_EVB14GHz	Y
X1	NX2520SA 50 MHz S1-2070-1010-10 (NDK)	NDK	NX2520SA	Y

1. Not populated

8 Reference documents

Table 2. Reference documents

Reference	Revision	Title
[1]	Latest version	Wideband RF/Microwave PLL fractional/integer frequency synthesizer with integrated VCOs and LDOs Datasheet. Document DM00235585 / 028443 (alternate)

9 Revision history

Table 3. Document revision history

Date	Revision	Changes
18-May-2017	1	Initial release. User manual derived from DB2797 (DocID028836 rev1 13-Jan-2016) with the following content updates: – *Figure 3: Disabling register polling* (GUI image) – *Figure 8: Main tab* – *Figure 9: PLL programming tab* – *Figure 10: Linear power regulator settings tab* – *Figure 15: STuW81300-EVB analog, RF and main signals* – *Figure 16: STuW81300-EVB power supply* – *Figure 17: STuW81300-EVB interface* – *Figure 18: STuW81300-EVB more analog, RF and optional signals* – *Table 1: STuW81300-EVAL BOM v2.0*.